Solid State TECHNOLOGY
Insights for Electronics Manufacturing

Process Watch: Baseline yield predicts baseline reliability

By David W. Price, Douglas G. Sutherland and Jay Rathert

Author's Note: *The Process Watch series explores key concepts about process control—defect inspection, metrology and data analysis—for the semiconductor industry. This article is the second in a five-part series on semiconductors in the automotive industry. In the first article, we introduced some of the challenges involved in the automotive supply chain and showed that the same defects that cause yield loss are also responsible for reliability issues. In this article, we discuss the connection between baseline yield and baseline reliability and present ways that both can be improved.*

The strong correlation between semiconductor IC yield and reliability has been well studied and documented. The data shown in figure 1 demonstrates this relationship. Similar outcomes have been shown at the lot, wafer and die location level. Simply put, when yield is high, reliability follows suit. As discussed in the first article of the Process Watch Automotive series, this yield-reliability correlation is not unexpected, since the defect types that cause die failures are the same as those that cause early reliability problems. Yield and reliability defects differ primarily by their size and where they occur on the device pattern in the die.

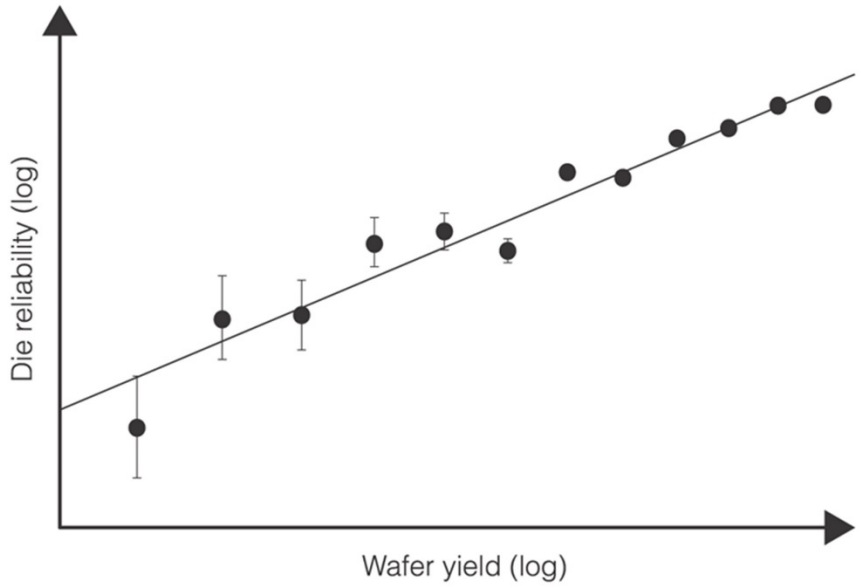

Figure 1. Data demonstrating the strong correlation between IC device reliability and yield.[1]

It follows that reducing the number of yield-killing defects in the IC manufacturing process will increase baseline yield and simultaneously increase device reliability in the field. Recognizing this fact, fabs serving the automotive market are faced with two critical questions. The first is economic in nature: what is the appropriate level of investment of time, money and resources in yield improvement to create the needed reliability gains? The second question is technical: what are the best defect reduction methodologies for boosting the baseline yield to the necessary levels?

For fabs that make consumer devices (ICs for mobile phones, tablets, etc.), “mature yield” is defined as the point where further improvements in yield no longer warrant the investment of time and resources. As a product matures, yield tends to stabilize at some high value, but usually well below 100%. Instead of pursuing higher yield, it makes more economic sense for the consumer fab to reallocate resources to developing the next design node’s processes and devices, or to reducing costs to improve the profitability of their legacy node.

For automotive fabs, the economic decision on whether to invest more to increase yield extends beyond the typical marginal revenue determination. When there is a reliability issue, the automotive IC manufacturer will likely bear the cost of expensive and time-consuming failure analysis, and will be held financially liable for field warranty failures, recalls and potential legal liabilities. Given that automotive IC reliability requirements are as much as two to three orders of magnitude higher than consumer IC

requirements, automotive fabs must achieve higher baseline yield levels. This requires a new way of thinking about what constitutes “mature yield.”

Figure 2 highlights the difference in mature yield between consumer and automotive fabs. As either type of fab moves up the yield curve, almost all systematic sources of yield loss have been resolved. The remaining yield loss is primarily due to random defectivity, contributed by either the process tools or the environment. A consumer fab may adopt a “good enough” approach to yield and reliability at this point. However, in the automotive industry, fabs employ a continuous improvement strategy to push the yield curve even higher. By driving down the incidence of yield-limiting defects, automotive fabs also reduce latent reliability defects, thereby optimizing their profits and mitigating risk.

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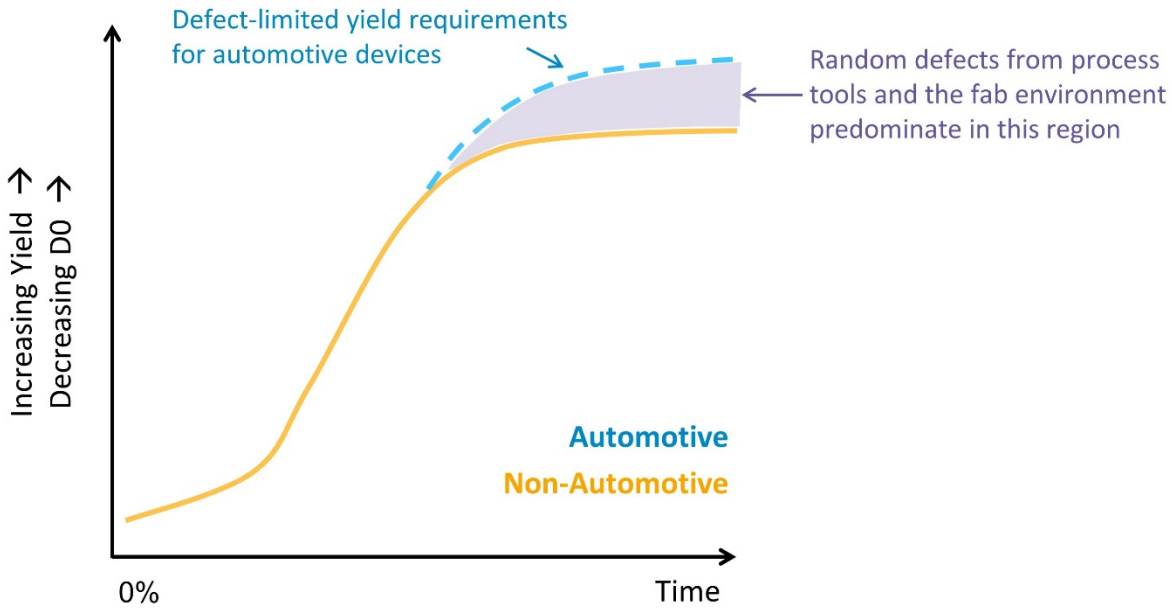

Figure 2. In a consumer device fab (yellow line), the top of the yield curve (Yield versus Time) is limited by diminishing returns to profitability for increased investment in defect reduction. The automotive fab yield curve, shown by the blue dashed line, also factors in reliability. Additional improvement to baseline yield must be made by automotive fabs to meet the parts per billion quality requirements. The purple shaded area highlights the difference in yield between consumer and automotive fabs – a difference that’s primarily related to process tool defectivity.

The automotive supply chain – from OEMs to Tier 1 suppliers to IC manufacturers – is adopting a mindset that “every defect matters” in pursuit of a Zero Defect strategy. They recognize that when latent defects escape the fab, the cost of discovery and mitigation increases as much as 10x at every additional level of the supply chain. As such, the existing over-reliance on electrical test needs to be replaced by a strategy where latent failures are stopped in the fab where the cost is lowest. Only by implementing a methodical

defect reduction program will a fab move towards the Zero Defect goal and be able to pass the stringent audits required by automobile manufacturers.

In addition to robust inline defect control capability, some of the defect reduction methods that automotive purchasing managers look for include:

- Continuous Improvement Program (CIP) for baseline defect reduction
- Golden Tool Work Flow
- Dog Tool Programs

Continuous Improvement in Baseline Defect Reduction

The foundation of any rigorous baseline defect reduction plan is the inline defect strategy. To successfully detect the defects that affect yield and reliability of their design rules and device types, a fab's inline defect strategy must include both an appropriate process control toolset and an adequate sample plan. The defect inspection systems utilized must produce the required defect sensitivity, be maintained to specifications and utilize well-tuned inspection recipes. The sample plan must be set for the right process steps at sufficient frequency to quickly flag process or tool excursions. Additionally, there should be sufficient inspection capacity to support a control plan that expedites excursion detection, root cause isolation and WIP-at-risk traceability. With these elements, an automotive fab should achieve a successful baseline defect reduction plan that can demonstrate positive yield trends over time, provide goals for further improvement, and equal industry best practices.

Within a baseline defect reduction plan, one of the biggest challenges is answering the question: where did this defect come from? The answer is often not straightforward. Sometimes the defect is detected many process steps away from the defect source. Sometimes the defect becomes apparent only after the wafer has gone through several other process steps that "decorate" it – i.e., make it more visible to inspection systems. A Tool Monitoring strategy helps resolve the question surrounding a defect's origin.

In Tool Monitoring / Tool Qualification (TMTQ) applications, a bare wafer is inspected, run through a specific process tool (or chamber) and then inspected again (figure 3). Any new defects found on the wafer with the second inspection must have been added by that specific process tool. The results are unequivocal; there is no question about the defect's origin. Automotive fabs pursuing a Zero Defect standard recognize the benefit of a Tool Monitoring strategy: with sensitive inspection recipes, appropriate control limits and out-of-control action plans (OCAP), the sources of random yield loss contributed by each process tool can be revealed and addressed.

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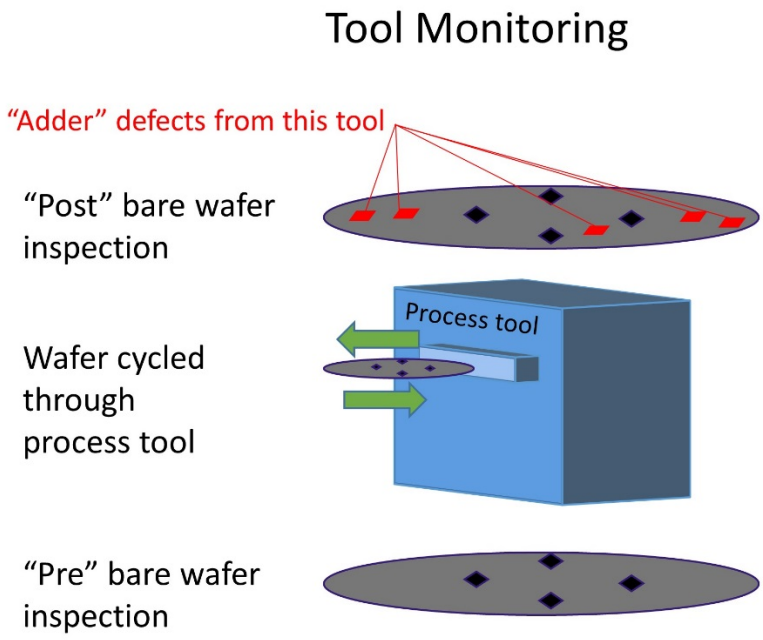

Figure 3. After baselining the bare wafer with a “pre” inspection, it can be cycled through some or all process tool steps. The “post” inspection reveals defects added by the process tool.

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Furthermore, when a process tool’s contribution of adder defects is plotted over time, as in figure 4, it provides a record of continuous improvement that can be audited and used to set future defect reduction goals. The defects from every tool in the fab can be classified to generate a defect library that can be referenced for failure analysis of field returns. This approach requires very frequent tool qualification – at

least once per day – and is usually used in conjunction with a Golden Tool Work Flow or Dog Tool Programs, discussed below.

Golden Tool Work Flow

A Golden Tool Work Flow is another strategy used by fabs to reach the Zero Defect standard required by the automotive industry. With a Golden Tool Work Flow or Automotive Work Flow (AWF), the wafers for automotive ICs only go through the best process tools in the fab, requiring that the fab knows the best tool for any given process step. To reliability determine which tool is best, fabs leverage data from inline and tool monitoring inspections, and then only use those tools for the Automotive Work Flow. Restricting automotive wafers to a single tool at each process step can lead to longer cycle times. However, this is usually preferable to sending automotive wafers through process flows that suffer from higher defect levels that can lead to reliability issues. When coupled with a methodical continuous improvement program, most fabs can usually get multiple tools qualified for AWF at each step by setting quarterly targets for defect reduction.

Because it is a difficult method the scale up, the Golden Tool Work Flow is best suited for fabs where only a small percentage of WIP is automotive. For fabs in high volume automotive production, a more methodical continuous improvement program, such as the Dog Tool approach described below, is preferred.

Dog Tool Programs

A Dog Tool Program is the opposite of a Golden Tool Work Flow as it proactively addresses the worst process tool – the dog tool – at any given process step. Fabs that have been most successful in driving down baseline defectivity often have done so by adopting a Dog Tool Program. They first take down the dog tool at every process step and work on that tool until it is better than the average of the remaining tools in that set. They repeat this process over and over until all tools in the set meet some minimum standard. An effective Dog Tool program requires that the fab has a methodical Tool Monitoring strategy to qualify each process tool at each step. At a minimum, this qualification procedure should be done daily on each tool to ensure there is sufficient data so that an ANOVA or Kruskal-Wallis analysis can identify the best and worst tools in each set. A Dog Tool Program, with planned process tool downtime, is the one of the fastest ways known to bring an entire fab up to automotive standards. By increasing yield and reliability, this strategy ultimately improves an automotive fab's effective capacity and profitability.

Summary

Automotive manufacturers who demand high reliability often require the fab to change their mindset about what really defines mature yield. In this article we have discussed several ways that fabs can reduce their

baseline defectivity and improve reliability and yield. In the next article in this series we will discuss some of the technical considerations regarding the sensitivity of defect inspection tools and how that helps ensure chip reliability

***About the Authors*:**

Dr. David W. Price and Jay Rathert are Senior Directors at KLA-Tencor Corp. Dr. Douglas Sutherland is a Principal Scientist at KLA-Tencor Corp. Over the last 15 years, they have worked directly with over 50 semiconductor IC manufacturers to help them optimize their overall process control strategy for a variety of specific markets, including automotive reliability, legacy fab cost and risk optimization, and advanced design rule time-to-market BKMs. The Process Watch series of articles attempts to summarize some of the universal lessons they have observed through these engagements.

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1. Mann, “Wafer Test Methods to Improve Semiconductor Die Reliability,” *IEEE Design & Test of Computers*, vol. 25, pp. 528-537, November-December 2008. https://doi.org/10.1109/MDT.2008.174
2. Price, Sutherland and Rathert, “Process Watch: The (Automotive) Problem With Semiconductors,” *Solid State Technology*, January 2018.

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